Sub Word Parallelism (SWP) for Multimedia Operator Design

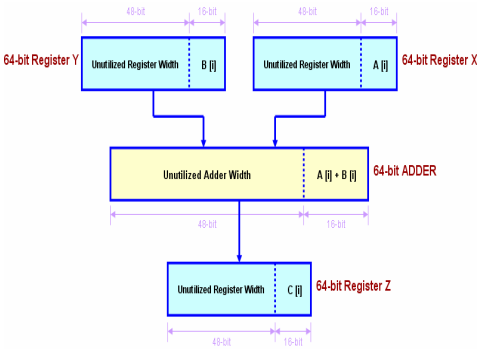
Shafqat Khan, Emmanuel Casseau, Daniel Menard

IRISA Lab./CAIRN – CNRS UMR 6074, Lannion, France

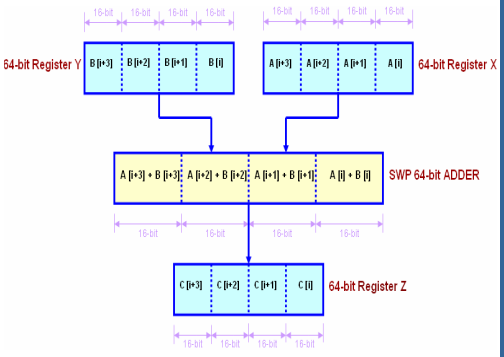
Sub Word Parallelism (SWP)

- Processors are optimized to perform operations on words of data (32 or 64 bits etc.)
- Multimedia applications perform computations on low precision data (8, 10, 12, 16 bits etc)

  ⇒ under utilization of resources for multimedia applications.
- SWP allows more than one computation using same datapath and operators.
- SWP partition operand into multiple lower precision subwords.
- Same operation on multiple sets of subwords in parallel .



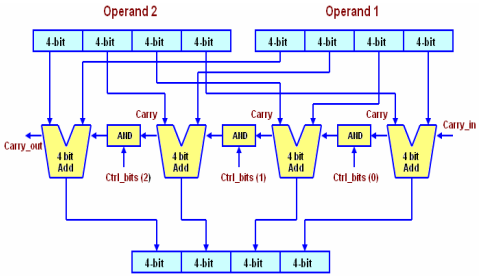
Architecture without SWP Capability



Architecture with SWP Capability

SWP ADD Operator

- SWP enable operators are required for SWP processor.
- In SWP, ADD blocking/unblocking of carry chain is done.
- 4-bit adder can be of any type like RCA, CLA etc.



SWP Enabled Adder Architecture

- Synthesis of simple and SWP enable adder using:
  - ASIC (130nm from ST and 90nm from UMC)
  - FPGA (Xilinx Virtex II)
- Simple 16-bit adder can perform:
  - One (16 + 16)
- SWP enable 16-bit adder can perform either :
  - Four (4 + 4) or
  - Two (8 + 8) or
  - One (16 + 16)

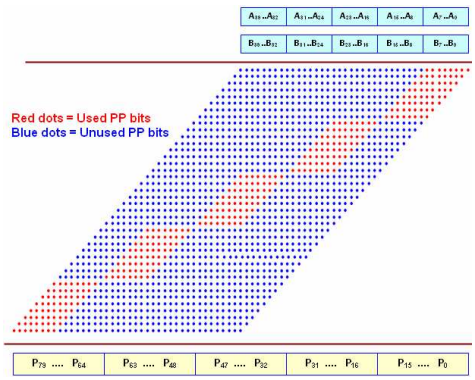
		90nm CMOS ASIC			130nm CMOS ASIC			FPGA VirtexII		
		Nand Gates	CP (ns)	Gates x CP	Nand Gates	CP (ns)	Gates x CP	CLBs	CP (ns)	CLBs x CP
16-bit RCA	Simple	118	1.07	126	114	3.20	365	34	12.9	439
	SWP	***123***	1.05	**129**	***122***	3.05	372	30	13.8	414
	Overhead (%)	4	-2	2	7	-5	2	-12	7	-6
16-bit CLA	Simple	168	0.65	109	175	1.41	247	33	12.1	399
	SWP	218	0.87	190	238	***1.54***	367	44	8.85	389
	Overhead (%)	30	34	74	36	9	49	33	-27	-3
16-bit Group CLA	Simple	153	0.92	141	149	1.87	279	32	8.82	282
	SWP	165	***0.86***	142	165	2.07	**342**	***29***	***8.75***	**254**
	Overhead (%)	8	-7	1	11	11	23	-9	-1	-10

Synthesis results for the 16-bit Adder

- Lower (gate x Critical path) means higher efficiency.
- SWP designs with minimum area and CP in bold blue.
- Efficiency of SWP Group CLA is higher (in bold black).
- Group CLA implements CLA in groups of 4-bits.

SWP MULTIPLY Operator

- Simultaneous multiplication of packed subwords.
- Conventional and Booth SWP multipliers are not efficient.
- Unused partial products (PPs) bits are made zeros.
- Subword products are concatenated to get final product.



SWP 40-bit Multiplier with subword size of 8-bit

- Simple 40-bit multiplier can perform:
  - One 40 x 40
- SWP 40-bit multiplier can perform either:
  - Five 8 x 8 or
  - Four 10 x 10 or
  - Three 12 x 12 or
  - Two 16 x 16 or
  - One 40 x 40.
- Both can perform signed/unsigned multiplication.

		90 nm CMOS ASIC			130 nm CMOS ASIC			FPGA VirtexII		
		Nand Gates	CP (ns)	Gates x CP	Nand Gates	CP (ns)	Gates x CP	CLBs	CP (ns)	CLBs x CP
40-bit Mult	Simple	14518	6.07	88124	10532	14.0	147448	917	19.7	18065
	SWP	15099	7.38	111431	11081	15.0	166215	1505	21.4	32207
	Overhead (%)	4	22	26	5	7	13	64	9	78

Synthesis results for the 40-bit Multiplier

- Efficient generation and arrangement of PPs results in low SWP overheads.
- Maximum SWP area overhead on ASIC is only 5%.
- Maximum SWP CP overhead is 22%.
- High CLBs overhead shows that design better suits ASIC.

SWP MAC Operator

- Most frequently used block in multimedia and DSP.
- MAC is used to perform:
  - Multiplication of two N-bit numbers.
  - Addition of 2N-bit product with 2N-bit addend.
- Simple 40-bit MAC can perform:
  - {a(40-bit) x b(40-bit)} + {c(80-bit)}
- SWP 40-bit MAC can perform either:
  - Five {a(8-bit) x b(8-bit)} + {c(16-bit)} or
  - Four {a(10-bit) x b(10-bit)} + {c(20-bit)} or
  - Three {a(12-bit) x b(12-bit)} + {c(24-bit)} or
  - Two {a(16-bit) x b(16-bit)} + {c(32-bit)} or
  - One {a(40-bit) x b(40-bit)} + {c(80-bit)}

		90 nm CMOS ASIC			130 nm CMOS ASIC			FPGA VirtexII		
		Nand Gates	CP (ns)	Gates x CP	Nand Gates	CP (ns)	Gates x CP	CLBs	CP (ns)	CLBs x CP
40-bit MAC	Simple	15163	6.14	93101	10967	14.3	156828	958	19.7	18873
	SWP	17238	9.17	158072	13019	18.5	240852	1778	27.3	48539
	Overhead (%)	14	49	70	19	30	54	86	39	157

Synthesis results for the 40-bit MAC

- SWP overheads for MAC are higher than multiplier:
  - In MAC both multiplier and adder need SWP capability.
  - Overheads of multiplier and adder accumulates in MAC.
- On ASIC maximum SWP area overhead is 19%.

Conclusion

- SWP improves processor's performance for multimedia and DSP applications.
- SWP increases efficiency through parallel execution of data.
- SWP provides flexibility at the cost of some area and CP increase.
- Multimedia applications also requires operators like:
  - Sum of absolute difference (SAD)
  - Sum of squared difference (SSD)
  - Accumulator (ACC)
  - Absolute (ABS)
- Work on multimedia oriented operators is in progress.

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